What is claimed is:

1. A system for measuring package interconnect impedance, said system comprising: a tester; a device under test (DUT)/load board which is configured to retain a substrate, said DUT/load board being connected to the tester, said tester being connected to a Digital Sampling Oscilloscope (DSO), said DSO configured to launch a signal which is received by the substrate, said DSO configured to receive a reflected signal from the substrate and provide the reflected signal to the tester, wherein the tester is configured to analyze the reflected signal and provide interconnect impedance versus time data.

2. A system as recited in claim 1, further comprising a probe card mounted to the tester, wherein the probe card contacts the substrate.

3. The system as recited in claim 1, wherein said tester includes a test head.

4. The system as recited in claim 2, wherein said probe card is mounted to the test head.

5. The system as recited in claim 2, wherein the probe card has probe pins.

6. The system as recited in claim 5, wherein probe pins from the probe card make contact with bump pads on the substrate.

7. The system as recited in claim 1, wherein said DUT/load board has a socket which is configured to hold said substrate.

8. The system as recited in claim 2, further comprising a coaxial cable which connects said DSO to said test head, wherein during testing, a signal is

launched using the DSO into a coaxial cable which is connected to the test head.

9. The system as recited in claim 1, further comprising a GPIB cable which connects said DSO to said tester, wherein the launched signal and the reflected signal are captured back by the DSO, and then fed into the tester via GPIB connections.

10. The system as recited in claim 1, further comprising post processing software which is configured to obtain interconnect impedance versus time information.

11. The system as recited in claim 2, wherein the probe card is fully populated to meet the bump pads on the substrate, wherein all except one pin are grounded.

12. The system as recited in claim 5, wherein the tester head is configured to select the probe pin that is going to be the signal in the probe card and makes the rest of the pins ground.

13. The system as recited in claim 12, wherein the test head is configured to let the DSO signal out the selected probe pin and is configured to allow a reflection from the DUT to get back to the DSO.

14. The system as recited in claim 12, wherein the test head is configured to obtain a waveform and store the data in a file.

15. A method for measuring package interconnect impedance, said method comprising: providing a tester; providing a device under test (DUT)/load board which is configured to retain a substrate, said DUT/load board being

connected to the tester, said tester being connected to a Digital Sampling Oscilloscope (DSO); using said DSO to launch a signal which is received by the substrate, wherein said DSO is configured to receive a reflected signal from the substrate and provide the reflected signal to the tester; and using post processing software to analyze the reflected signal and provide interconnect impedance versus time data.

16. The method as recited in claim 15, further comprising providing a probe card mounted to the tester, wherein the probe card contacts the substrate.

17. The method as recited in claim 15, wherein said tester includes a test head.

18. The method as recited in claim 16, wherein said probe card is mounted to the test head.

19. The method as recited in claim 16, wherein the probe card has probe pins.

20. The method as recited in claim 19, wherein probe pins from the probe card make contact with bump pads on the substrate.

21. The method as recited in claim 15, wherein said DUT/load board has a socket which is configured to hold said substrate.

22. The method as recited in claim 16, wherein said DUT/load board has signal wires which are connected to the tester, said method further comprising providing a coaxial cable which connects said DSO to said test head, wherein during testing, a signal is launched using the DSO into a coaxial cable which is connected to the test head.

23. The method as recited in claim 15, further comprising providing a GPIB cable which connects said DSO to said tester, wherein the launched signal

and the reflected signal are captured back by the DSO, and then fed into the tester via GPIB connections.

24. The method as recited in claim 16, wherein the probe card is fully populated to meet the bump pads on the substrate, wherein all except one pin are grounded.

25. The method as recited in claim 19, wherein the test head is configured to select the probe pin that is going to be the signal in the probe card and makes the rest of the pins ground.

26. The method as recited in claim 25, wherein the test head is configured to let the DSO signal out the selected probe pin and is configured to allow a reflection from the DUT to get back to the DSO.

27. The method as recited in claim 25, wherein the test head is configured to obtain a wave form and store the data in a file.